WHAT IS CLAIMED IS:

1. A method of driving a display device, said display device having a plurality of pixels in a matrix comprising n rows and m columns,

in accordance with a partial display instruction, said display device performing a desired partial display on a partial display area formed of pixels of s rows by m columns, where s is a desired value, and said display device displaying a background on a remaining background area of said matrix comprising n rows and m columns; wherein:

during one frame in a partial display mode,

partial display data is written into each pixel of said s row by m column partial display area; and

background display data is written into pixels of an area of k rows by m columns in said background area;

wherein each of n, m, s, and k is an integer greater than 1 and $s < n$ and $k < n$.

2. A method of driving a display device defined in Claim 1, wherein row to be selected associated with pixels of said area of k rows by m columns in said background area is shifted every one frame.

3. A method of driving a display device defined in Claim 2, wherein said background display data is written into each pixel in said background area over a total ((n-s)/k) frame

duration.

4. A method of driving a display device defined in Claim 2, wherein said background display data is written into each pixel in said background area over a total ((n-s)/k) frame duration;

polarities of said background display data are inverted with respect to a reference potential, and inverted background display data is written into pixels in the same row over a next total ((n-s)/k) frame duration.

5. A method of driving a display device defined in Claim 1, wherein rows other than the k rows selected during one frame in said background display area are inhibited from being selected.

6. A method of driving a display device defined in Claim 1, wherein when said partial display instruction is issued,

a pixel clock is used as a unit clock, a frequency of said pixel clock being lower than that of a pixel clock used as a unit clock for selecting and normally displaying all pixels of said matrix comprising n rows and m columns during one frame;

said partial display data is written into all pixels in said partial display area; and

said background display data is written into pixels of said area of k rows by m columns in said background display

area.

7. A method of driving a display device defined in Claim 6, wherein

a transfer rate of a row selection pulse is increased, when said partial display instruction is issued, and arrival of a selection duration of rows other than those of said area of k rows by m columns in said background display area is detected.

8. A method of driving a display device defined in Claim 1, wherein

said background display data is written to all pixels of said matrix comprising n rows and m columns after said partial display instruction has been issued;

said partial display data is sequentially written into pixels of said area of s rows by m columns, and background display data is written into pixels of said area of k rows by m columns.

9. A method of driving a display device defined in Claim 1, wherein said background display data comprises off-display data or arbitrary background color data.

10. A method of driving a display device defined in Claim 1, wherein said display device comprises a liquid crystal device.

11. A method of driving a display device, said display device having a plurality of pixels in a matrix comprising n rows and m columns,

in accordance with a partial display instruction, said display device performing a partial display on a partial display area formed of an s row by m column matrix, where s is a desired value, and said display device displaying a background on a remaining background area; wherein

during one frame in a partial display mode, predetermined partial display data is sequentially written into each pixel of said partial display area; and

background display data is written into pixels of the (s+1)-th row area next to the final row in said partial display area and into pixels of an area of k rows by m columns, within said background area;

where each of n, m, s, and k is an integer greater than 1 and $s < n$ and $k < n-s-1$.

12. A method of driving a display device defined in Claim 11, wherein row to be selected associated with pixels of said area of k rows by m columns in said background area is shifted every one frame.

13. A method of driving a display device defined in Claim 12, wherein said background display data is written into pixels of an area of (n-s-1) rows by m columns in said background display area over a total ((n-s-1)/k) frame duration.

14. A method of driving a display device defined in Claim 12, wherein

said background display data is written into pixels of said area of (n-s-1) rows by m columns in said background display area over a total ((n-s-1)/k) frame duration;

polarities of said background display data are inverted with respect to a reference potential, and inverted background display data is written into pixels in the same row in a next total ((n-s-1)/k) frame duration.

15. A method of driving a display device defined in Claim 11, wherein

when said partial display instruction is issued,

a pixel clock is used as a unit clock, a frequency of said pixel clock being lower than that of a pixel clock used as a unit clock for selecting and normally displaying all pixels of said matrix comprising n rows and m columns during one frame;

said partial display data is written into all pixels in said partial display area; and

said background display data is written into pixels of said (s+1)-th row area and pixels of said area of k rows by m columns, in said background display data.

16. A method of driving a display device defined in Claim 11, wherein

said background display data is written into all pixels

of said matrix comprising n rows and m columns after said partial display instruction has been issued;

said partial display data is sequentially written into pixels of said area of s rows by m columns; and background display data is written into pixels of said (s+1)-th pixel and pixels of said area of k rows by m columns.

17. A method of driving a display device defined in Claim 11, wherein

during the next first frame when said partial display instruction is detected,

said partial display data is sequentially written into each pixel in said partial display area formed of said s row by m column matrix, and said background display data is sequentially written into all pixels of said background area;

during each frame after a second frame following said first frame,

said partial display data is written into each pixel in said partial display area formed of said s row by m column; and said background display data is written into pixels of the (s+1)-th row area and pixels of said area of k rows by m columns in said background area.

18. A method of driving a display device defined in Claim 11, wherein said background display data comprises off-display data or arbitrary background color data.

19. A method of driving a display device defined in Claim 11, wherein said display device comprises a liquid crystal device.

20. A method of driving a display device, said display device having a plurality of pixels in a matrix comprising n rows and m columns,

in accordance with a partial display instruction, said display device performing a desired partial display on a partial display area formed of pixels of area of s rows by m columns, where s is a desired value, and said display device displaying a background on a remaining background area of said matrix comprising n rows and m columns; wherein:

during a first frame over which said partial display instruction is detected and a normal display mode changes to a partial display mode,

predetermined partial display data is sequentially written into each pixel of said partial display area of s rows by m columns; and background display data is sequentially written into pixels of said background area;

during each frame after the second frame following the first frame in a partial display mode,

said partial display data is written into each pixel of said area of s rows by m columns partial display area; and

said background display data is written into pixels of said area of k rows by m columns in said background area;

wherein each of n, m, s, and k is an integer more than 1 and $s < n$ and $k < n-s$.

21. A method of driving a display device defined in Claim 20, wherein row to be selected associated with pixels of said area of k row by m columns in said background area is shifted every one frame.

22. A method of driving a display device defined in Claim 21, wherein said background display data is written into all pixels in said background area over a total (n-s)/k frame duration after said second frame.

23. A method of driving a display device defined in Claim 21, wherein rows other than the k row in said background area selected during one frame after the second frame are inhibited from being selected.

24. A method of driving a display device defined in Claim 20, wherein:

during each frame after the second frame,

a pixel clock is used as a unit clock, a frequency of said pixel clock being lower than that of a pixel clock used as a unit clock for selecting and normally displaying all pixels of said matrix comprising n rows and m columns during one frame;

said partial display data is written into all pixels in said partial display area; and

said background display data is written into pixels of

said area of k rows by m columns in said background display area.

25. A method of driving a display device defined in Claim 20, wherein said background display data comprises off-display data or arbitrary background color data.

26. A method of driving a display device defined in Claim 20, wherein said display device comprises a liquid crystal device.

27. A drive circuit for a display device, said display device having a plurality of pixels in a matrix comprising n rows and m columns, and said plurality of pixels are selected every row line and display display data supplied from a column line,

when a partial display instruction is issued, during one frame, said display device selects pixels in an area of s rows by m columns in said matrix comprising n rows and m columns, sequentially writes predetermined partial display data, selects pixels in an area of k rows by m columns in a remaining background area in said matrix comprising n rows and m columns, and writes background display data, said drive circuit comprising:

a row clock generator for generating a row clock corresponding to a row selection duration of each row;

a row clock counter for counting a row clock every one frame;

a partial display row detector for detecting an incoming timing for s rows to which said partial display data is written;

a background display row detector for detecting an incoming timing for a k row to which background display data is written during said one frame; and

a driver control signal generator for producing a driver control signal when said partial display row detector or said background display row detector detects an arrival of a row to be displayed, said driver control signal allowing a row driver driving said matrix comprising n row and m columns every row to perform a row drive operation;

wherein each of n, m, s and k is an integer greater than 1 and s <n and k < n.

28. A drive circuit for a display device defined in Claim 27, further comprising a frame counter for counting the number of frames, and wherein said background display row detector shifts row to which said background display data is written based on a count value counted by said frame counter.

29. A drive circuit for a display device defined in Claim 27, further comprising a polarity inverted signal generator for inverting a polarity of display data with respect to a predetermined reference voltage every unit duration; and wherein respective pixels in said background display area are respectively selected once over one background display

duration being a total (n-s)/k frame duration, and said polarity inverted signal generator detects an arrival of the next one background duration and inverts the polarity of said background display data.

30. A drive circuit for a display device defined in Claim 27, further comprising a frequency divider for dividing unit clocks used for selecting and normally displaying all pixels of said matrix comprising n rows by m columns; wherein

when said partial display instruction is issued, during one frame,

using as a unit clock divided pixel clocks from said frequency divider, said partial display data is controlled to write to pixels of said area of s rows by m columns and said background display data is controlled to write to pixels of said area of k rows by m columns.

31. A drive circuit for a display device defined in Claim 30, further comprising a row clock controller for detecting, based on a display row detection signal in said partial display row detector and said background row detector, an arrival of a selection duration of rows other than pixels of said area of k rows by m columns, and increasing the frequency of said row clock.

32. A drive circuit for a display device defined in Claim 27, further comprising a mode changeover timing controller for,

when an instruction for changing form a normal display mode to a partial display mode is issued, changing display data to all pixels of said matrix comprising n row by m columns to background display data in the next first frame of said instruction and starting said driver control signal generator to generate said driver control signal, from the next frame.

33. A method of driving a display device defined in Claim 27, wherein said background display data comprises off-display data or arbitrary background color data.

34. A method of driving a display device defined in Claim 27, wherein said display device comprises a liquid crystal device.

35. A drive circuit for a display device, said display device having a plurality of pixels in a matrix comprising n rows and m columns, and said plurality of pixels are selected every row line and display display data supplied from a column line,

when a partial display instruction is issued, during one frame,

said display device selects pixels in an area of s rows by m columns in said matrix comprising n rows and m columns, sequentially writes predetermined partial display data, selects pixels of (s+1)-th row and pixels of an area of k rows by m columns in the remaining background area within said matrix comprising n rows and m columns, and writes background display data, comprising:

a row clock generator for generating a row clock corresponding to a row selection duration of each row;

a row clock counter for counting a row clock every one frame;

a partial display row detector for detecting an incoming timing for s rows to which said partial display data is written;

a background display row detector for detecting an incoming timing for the (s+1)-th row and k row to which background display data is written during said one frame; and

a driver control signal generator for producing a driver control signal when said partial display row detector or said background display row detector detects an arrival of a row to be displayed, said driver control signal allowing a row driver driving said a matrix comprising n rows and m columns every row to perform a row drive operation,

wherein each of n, m, s, and k is an integer more than 1 and s <n and k < n-s-1.

36. A drive circuit for a display device defined in Claim 35, further comprising a frame counter for counting the number of frames, and wherein

said background display row detector shifts row to which said background display data is written based on a count value counted by said frame counter.

37. A drive circuit for a display device defined in Claim 35,

further comprising a polarity inverted signal generator for inverting a polarity of display data with respect to a predetermined reference voltage every unit duration, and wherein

respective pixels in said background display area, except pixels associated with said (s+1)-th row, are respectively selected once over one background display duration being a total (n-s-1)/k frame duration, and said polarity inverted signal generator detects an arrival of the next one background duration and inverts the polarity of said background display data.

38. A drive circuit for a display device defined in Claim 35, further comprising a frequency divider for dividing unit clocks used for selecting and normally displaying all pixels of said matrix comprising n rows and m columns during one frame; wherein

when said partial display instruction is issued, during one frame,

using as a unit clock divided pixel clocks from said frequency divider, said partial display data is controlled to write to pixels of said area of s rows by m columns and said background display data is controlled to write to pixels of (s+1)-th row and said area of k rows by m columns.

39. A drive circuit for a display device defined in Claim 38, further comprising a row clock controller for detecting, based

on a display row detection signal in said partial display row detector and said background row detector, an arrival of a selection duration of rows other than pixels associated with the (s+1)-th row and pixels of said area of k rows by m columns , and increasing the frequency of said row clock.

40. A method of driving a display device defined in Claim 35, wherein said background display data comprises off-display data or arbitrary background color data.

41. A method of driving a display device defined in Claim 35, wherein said display device comprises a liquid crystal device.

42. A drive circuit for a display device, wherein said display device having a plurality of pixels in a matrix comprising n rows and m columns, and said plurality of pixels are selected every row line and display display data supplied from a column line,

when a partial display instruction is issued, during one frame,

said display device selects pixels in an area of s rows by m columns in said matrix comprising n rows and m columns, sequentially writes predetermined partial display data, selects pixels from an area of k rows and m columns in the remaining background area within said matrix comprising n rows and m columns, and writes background display data, comprising:

a row clock generator for generating a row clock

corresponding to a row selection duration of each row;

a row clock counter for counting a row clock every one frame;

a partial display row detector for detecting an incoming timing for s rows to which said partial display data is written;

a background area detector for detecting an incoming timing for the leading row and the final row of said background area;

a background display row detector for detecting an incoming timing for k rows to which background display data is written during one frame in a partial display mode;

a data output controller for allowing partial display data to be output for the duration over said partial display row detector detects an arrival of a row to be displayed and for setting output display data to background display data for the duration over which said background area detector detects an arrival of the leading row and the final row in said background area, in the first frame in transition from a normal display mode to a partial display mode; and

a driver control signal generator for producing a driver control signal when said partial display row detector or said background display row detector detects an arrival of a row to be displayed after a second frame in transition to a partial display mode, said driver control signal allowing a row driver to perform a row drive operation,

wherein each of n, m, s, and k is an integer more than 1

and s <n and k < n-s.

43. A drive circuit for a display device defined in Claim 42, wherein said background display data comprises off-display data or arbitrary background color data.

44. A drive circuit for a display device defined in Claim 42, wherein said display device comprises a liquid crystal device.